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CMOS WITH STRAINED SILICON CHANNEL NMOS AND SILICON GERMANIUM CHANNEL PMOS

ABSTRACT OF THE DISCLOSURE

Conventional CMOS devices suffer from imbalance because the mobility of holes in the PMOS transistor is less than the mobility of electrons in the NMOS transistor. The use of strained silicon in the channels of CMOS devices further exacerbates the difference in electron and hole mobility, as strained silicon provides a greater increase in electron mobility than hole mobility. However, hole mobility is increased in the SiGe layer underlying the strained silicon layer. Therefore, a more evenly-balanced, high-speed CMOS device is formed by including strained silicon in the NMOS transistor and not in the PMOS transistor of a CMOS device.